REMARKS

Claims 15-26 stand rejected on double patenting grounds under 35 USC § 101 and under the judicially created doctrine against double patenting. Claims 15-18 and 20-25 stand rejected under 35 USC 103(a) as being obvious over US Pat. No. 4,888,300 (hereafter Burton) in view of Streetman, *Solid State Electronic Devices* and Wolf et al., *Silicon Processing for the VLSI Era*. Claims 19 and 26 stand rejected under 35 USC 103(a) as being obvious over Burton in view of Wolf and US Pat. No. 6,268,637 (hereafter Gardner). Applicant has amended claims 15-17, 19-21, and 26. In view of the amendments and arguments set forth below, Applicant submits that all pending claims are in condition for allowance.

PRIORITY

As this is a Divisional Application, the Examiner requested that the Applicant set forth the portion of the earlier disclosure that is germane to the invention as claimed in this Divisional Application. Because the Applicant is relying on the earlier disclosure in its entirety, the Applicant has amended the specification to note that the earlier disclosure is being incorporated herein by reference. This amendment is supported by the Transmittal that was originally filed with this application.

DOUBLE PATENTING

The Examiner has rejected claim 26 under 35 USC 101 as claiming the same invention as that of claim 12 of prior US Patent No. 5,972,758. Claim 26 has now been amended as noted above. The Applicant believes the amendments made to claim 26 are sufficient to overcome the double patenting rejection. In particular, amended claim 26 now recites:

> ...isotropically etching the first trench and the second trench with an etchant ... to form a first undercut region subjacent to the first trench and a second undercut

region subjacent to the second trench, wherein the first undercut region is isolated from the second undercut region by a portion of the semiconductor substrate....

Claim 12 of US Patent No. 5,972,758 does not disclose these limitations. As such, the Applicant believes that the double patenting rejection of claim 26 has been overcome.

The Examiner has also rejected claims 15-25 under the judicially created doctrine of double patenting over claims 1-11 of prior US Patent No. 5,972,758. Independent claim 15 has now been amended as noted above. The Applicant believes the amendments made to claim 15 are sufficient to overcome the double patenting rejection. In particular, amended claim 15 now recites:

...integrally forming a T-shaped pedestal in the semiconductor substrate by isotropically etching the exposed semiconductor substrate to form a first undercut region subjacent to the first trench and a second undercut region subjacent to the second trench, wherein a top portion of the T-shaped pedestal is disposed between the first trench and the second trench and a stem portion of the T-shaped pedestal is disposed between the first undercut region and the second undercut region....

Claims 1-11 of US Patent No. 5,972,758 do not disclose these limitations. As such, the Applicant believes that the double patenting rejection of independent claim 15, as well as dependent claims 16-25, has been overcome.

OBVIOUSNESS REJECTIONS UNDER 35 USC 103(a)

The Examiner has rejected claims 15-18 and 20-25 under 103(a) as being obvious over Burton in view of Streetman and Wolf. As noted above, the Applicant has amended these claims and believes the amended claims overcome the 103(a) rejections and are in condition for allowance.

Regarding independent claim 15, this claim has been amended to recite the following:

> ...integrally forming a T-shaped pedestal in the semiconductor substrate by isotropically etching the exposed semiconductor substrate to form a first undercut region subjacent to the first trench and a second undercut region subjacent to the second trench, wherein a top portion of the T-shaped pedestal is disposed between the first trench and the second trench and a stem portion of the T-shaped pedestal is disposed between the first undercut region and the second undercut region....

Burton does not disclose this limitation of claim 15. Rather, Burton teaches etching a single cavity below an epitaxial layer, where the cavity extends below the entire epitaxial layer and causes the epitaxial layer to become an island. The cavity therefore undercuts the portion of the epitaxial layer that will form the channel region of the transistor. As demonstrated in Figure 8 of Burton, the epitaxial layer "floats" atop the etched cavity. Simply stated, the cavity of Burton completely undercuts the channel region of the transistor and causes the entire transistor to float on a layer of polysilicon.

Contrary to this, claim 15 of the instant application recites etching two undercut regions below the trenches that are isolated from one another by a stem portion of the T-shaped pedestal (see, e.g., Figure 3(e) of the Applicant's disclosure). The two undercut regions are distinct and do not completely undercut the portion of the semiconductor substrate that will form the channel region of the transistor. In fact, the channel region is contiguous with the semiconductor substrate. The transistor, therefore, does not float atop the undercut regions.

The difference in Burton and in Applicant's claim 15 is easily seen by comparing Figure 8 of Burton to Figure 3(e) of the Applicant's disclosure. As will be clear to one of skill in the art, these two structures are completely different and provide completely different advantages and disadvantages. Accordingly, the Applicant submits that Burton cannot be used to support a 103(a) rejection of claim 15 as amended and requests that claim 15 be allowed.

Regarding dependent claims 16-25, the Applicant submits that these claims are in condition for allowance at least by way of their dependence on allowable base claim 15.

Regarding independent claim 26, this claim has been amended to recite the following:

> ...isotropically etching the first trench and the second trench with an etchant ... to form a first undercut region subjacent to the first trench and a second undercut region subjacent to the second trench, wherein the first undercut region is isolated from the second undercut region by a portion of the semiconductor substrate....

As discussed above, Burton teaches forming a single cavity under the entire epitaxial layer that will form a transistor. The Applicant's claim 26, on the other hand, teaches forming two undercut regions that are isolated from one another. As before, these two structures are completely different and provide completely different advantages and disadvantages. Accordingly, the Applicant submits that Burton cannot be used to support a 103(a) rejection of claim 26 as amended and requests that claim 26 be allowed.

CONCLUSION

Applicant submits that all claims now pending are in condition for allowance. Applicant reserves the right to argue the patentability of the dependent claims and currently believes that all claims are allowable at least by way of their dependence on an allowable base claim. Such action is earnestly solicited at the earliest possible date. If there is a deficiency in fees, please charge our Deposit Account No. 02-2666.

Applicant hereby requests a two-month extension of time in the accompanying petition, a check for which is included.

Respectfully submitted,

Date: October 19, 2005

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